# PCA9543A/43B

## 2-channel I²C-bus switch with interrupt logic and reset

Rev. 8 — 3 April 2014 Product data sheet

## 1. General description

The PCA9543A/43B is a bidirectional translating switch, controlled by the I²C-bus. The SCL/SDA upstream pair fans out to two downstream pairs, or channels. Any individual SCx/SDx channels or combination of channels can be selected, determined by the contents of the programmable control register. Two interrupt inputs, $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$, one for each of the downstream pairs, are provided. One interrupt output, $\overline{\text{INT}}$, which acts as an AND of the two interrupt inputs, is provided.

An active LOW reset input allows the PCA9543X to recover from a situation where one of the downstream I²C-buses is stuck in a LOW state. Pulling the $\overline{\text{RESET}}$ pin LOW resets the I²C-bus state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the $V_{DD}$ pin can be used to limit the maximum high voltage which will be passed by the PCA9543X. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

The PCA9543A and PCA9543B are identical except for the fixed portion of the slave address.

## 2. Features and benefits

- 1-of-2 bidirectional translating switches
- I²C-bus interface logic; compatible with SMBus standards
- 2 active LOW interrupt inputs
- Active LOW interrupt output
- Active LOW reset input
- 2 address pins allowing up to 4 devices on the I²C-bus
- Alternate address versions A and B allow up to a total of 12 devices on the bus for larger systems or to resolve address conflicts
- Channel selection via I²C-bus, in any combination
- Power-up with all switch channels deselected
- Low $R_{on}$ switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V

- 5 V tolerant inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO14, TSSOP14

# 3. Ordering information

**Table 1. Ordering information**

| Type number | Topside marking | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| PCA9543AD | PCA9543A | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| PCA9543APW | PA9543A | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| PCA9543BPW | PA9543B | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

## 3.1 Ordering options

**Table 2. Ordering options**

| Type number | Orderable part number | Package | Packing method | Minimum order quantity | Temperature |
|---|---|---|---|---|---|
| PCA9543AD | PCA9543AD,112 | SO14 | Standard marking * IC's tube - DSC bulk pack | 1140 | $T_{amb}$ = –40 °C to +85 °C |
| | PCA9543AD,118 | SO14 | Reel 13" Q1/T1 *standard mark SMD | 2500 | $T_{amb}$ = –40 °C to +85 °C |
| PCA9543APW | PCA9543APW,112 | TSSOP14 | Standard marking * IC's tube - DSC bulk pack | 2400 | $T_{amb}$ = –40 °C to +85 °C |
| | PCA9543APW,118 | TSSOP14 | Reel 13" Q1/T1 *standard mark SMD | 2500 | $T_{amb}$ = –40 °C to +85 °C |
| PCA9543BPW | PCA9543BPW,118 | TSSOP14 | Reel 13" Q1/T1 *standard mark SMD | 2500 | $T_{amb}$ = –40 °C to +85 °C |


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## 4. Block diagram

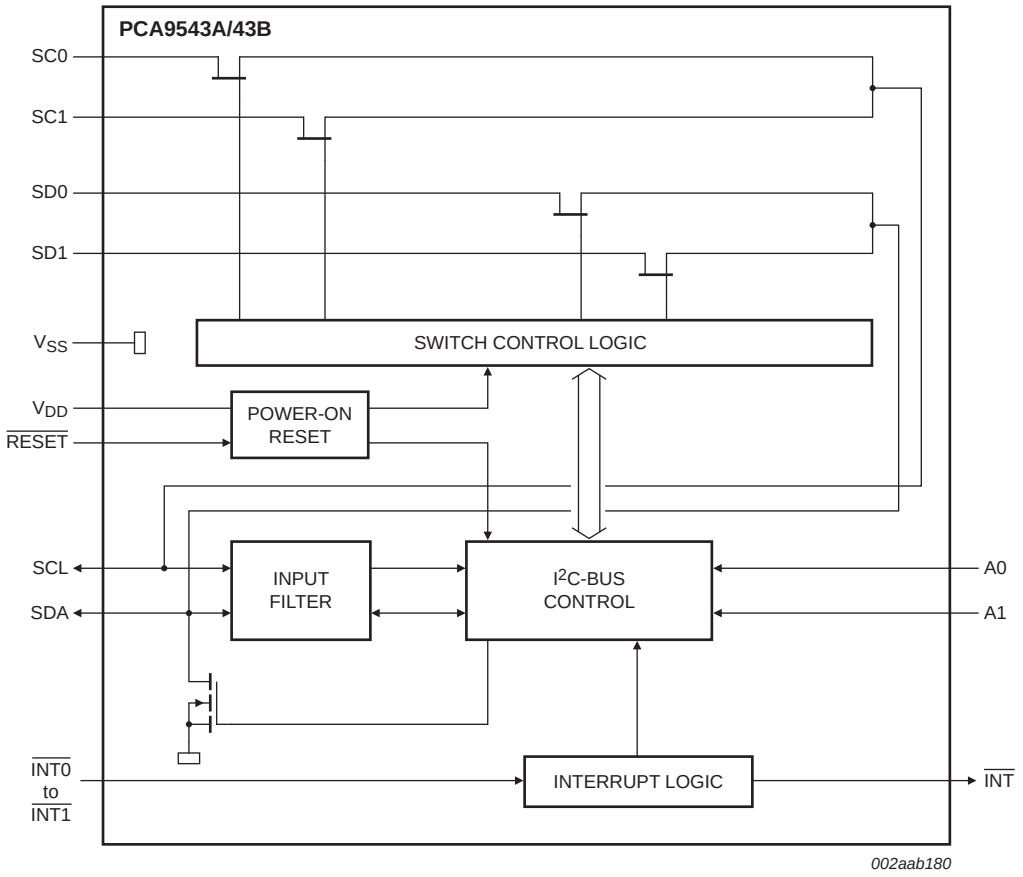



**Fig 1. Block diagram of PCA9543A/43B**


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# 5. Pinning information

## 5.1 Pinning

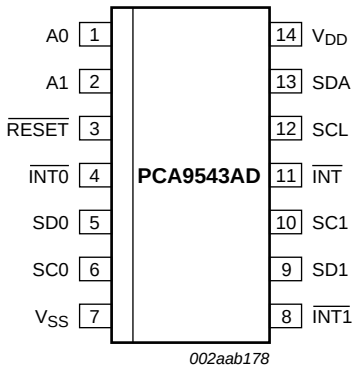



Fig 2. Pin configuration for SO14

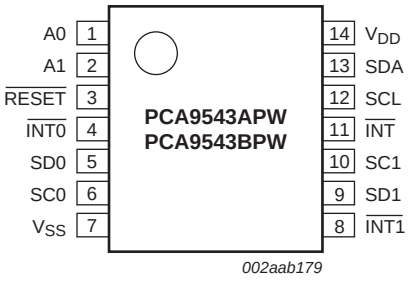



Fig 3. Pin configuration for TSSOP14

## 5.2 Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|---|---|---|
| A0 | 1 | address input 0 |
| A1 | 2 | address input 1 |
| $\overline{\text{RESET}}$ | 3 | active LOW reset input |
| $\overline{\text{INT0}}$ | 4 | active LOW interrupt input 0 |
| SD0 | 5 | serial data 0 |
| SC0 | 6 | serial clock 0 |
| $V_{SS}$ | 7 | supply ground |
| $\overline{\text{INT1}}$ | 8 | active LOW interrupt input 1 |
| SD1 | 9 | serial data 1 |
| SC1 | 10 | serial clock 1 |
| $\overline{\text{INT}}$ | 11 | active LOW interrupt output |
| SCL | 12 | serial clock line |
| SDA | 13 | serial data line |
| $V_{DD}$ | 14 | supply voltage |


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# 6. Functional description

Refer to Figure 1 “Block diagram of PCA9543A/43B”.

## 6.1 Device address

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9543A/43B is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

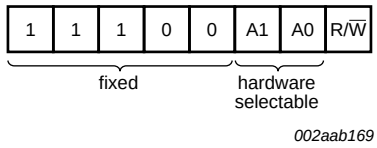



**Fig 4. Slave address PCA9543A**

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

The PCA9543B is an alternate address version, if needed for larger systems or to resolve address conflicts. The data sheet will reference the PCA9543A, but the PCA9543B functions identically except for the slave address.

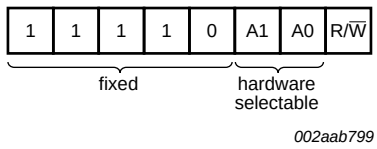



**Fig 5. Slave address PCA9543B**

### 6.1.1 Address maps

**Table 4. PCA9543A address map**

| Pin connectivity | | Address of PCA9543A | | | | | | | | Address byte value | | 7-bit hexadecimal address without R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | A0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Write | Read | |
| $V_{SS}$ | $V_{SS}$ | 1 | 1 | 1 | 0 | 0 | 0 | 0 | - | E0h | E1h | 70h |
| $V_{SS}$ | $V_{DD}$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | - | E2h | E3h | 71h |
| $V_{DD}$ | $V_{SS}$ | 1 | 1 | 1 | 0 | 0 | 1 | 0 | - | E4h | E5h | 72h |
| $V_{DD}$ | $V_{DD}$ | 1 | 1 | 1 | 0 | 0 | 1 | 1 | - | E6h | E7h | 73h |


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**Table 5. PCA9543B address map**

| Pin connectivity | | Address of PCA9543B | | | | | | | | Address byte value | | 7-bit hexadecimal address without R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | A0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Write | Read | |
| $V_{SS}$ | $V_{SS}$ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | - | F0h | F1h | 78h |
| $V_{SS}$ | $V_{DD}$ | 1 | 1 | 1 | 1 | 0 | 0 | 1 | - | F2h | F3h | 79h |
| $V_{DD}$ | $V_{SS}$ | 1 | 1 | 1 | 1 | 0 | 1 | 0 | - | F4h | F5h | 7Ah |
| $V_{DD}$ | $V_{DD}$ | 1 | 1 | 1 | 1 | 0 | 1 | 1 | - | F6h | F7h | 7Bh |

## 6.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9543A/43B, which will be stored in the control register. If multiple bytes are received by the PCA9543A/43B, it will save the last byte received. This register can be written and read via the I²C-bus.

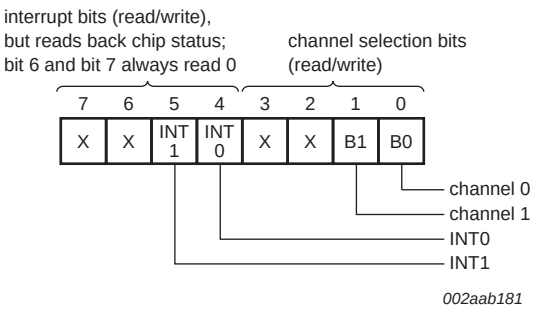



**Fig 6. Control register**

### 6.2.1 Control register definition

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9543A/43B has been addressed. The 2 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I²C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Bits INT0, INT1, D6 and D7 are all writable, but will read the chip status. INT0 and INT1 indicate the state of the corresponding interrupt input. D7 and D6 always read 0.
See Section 6.2.2.


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**Table 6. Control register: Write — channel selection; Read — channel status**

| D7 | D6 | INT1 | INT0 | D3 | D2 | B1 | B0 | Command |
|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | 0 | channel 0 disabled |
| | | | | | | | 1 | channel 0 enabled |
| X | X | X | X | X | X | 0 | X | channel 1 disabled |
| | | | | | | 1 | | channel 1 enabled |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | no channel selected; power-up/reset default state |

**Remark:** Channel 0 and channel 1 can be enabled at the same time. Care should be taken not to exceed the maximum bus capacitance.

### 6.2.2 Interrupt handling

The PCA9543A/43B provides 2 interrupt inputs, one for each channel, and one open-drain interrupt output. When an interrupt is generated by any device, it will be detected by the PCA9543A/43B and the interrupt output will be driven LOW. The channel need not be active for detection of the interrupt. A bit is also set in the control register.

Bit 4 and bit 5 of the control register corresponds to the $\overline{INT0}$ and $\overline{INT1}$ inputs of the PCA9543A/43B, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PCA9543A/43B and read the contents of the control register to determine which channel contains the device generating the interrupt. The master can then reconfigure the PCA9543A/43B to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to $V_{DD}$ through a pull-up resistor.

**Table 7. Control register: Read — interrupt**

| 7 | 6 | INT1 | INT0 | 3 | 2 | B1 | B0 | Command |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | X | 0 | X | X | X | X | no interrupt on channel 0 |
| | | | 1 | | | | | interrupt on channel 0 |
| 0 | 0 | 0 | X | X | X | X | X | no interrupt on channel 1 |
| | | 1 | | | | | | interrupt on channel 1 |

**Remark:** Two interrupts can be active at the same time. D6 and D7 always read 0.

## 6.3 $\overline{RESET}$ input

The $\overline{RESET}$ input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of $t_{w(rst)L}$, the PCA9543A/43B will reset its registers and I²C-bus state machine and will deselect all channels. The $\overline{RESET}$ input must be connected to $V_{DD}$ through a pull-up resistor.


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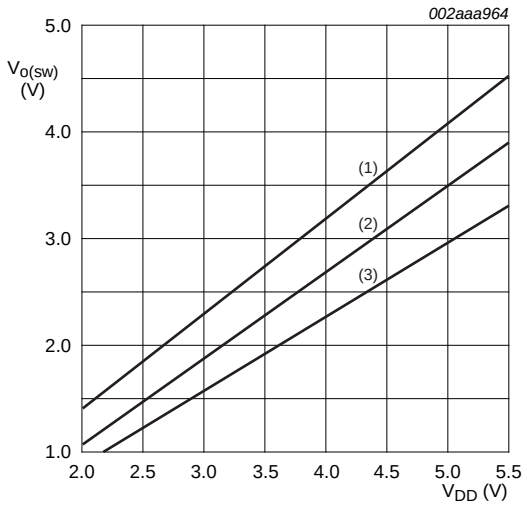
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## 6.4 Power-on reset

When power is applied to $V_{DD}$, an internal Power-On Reset (POR) holds the PCA9543A/43B in a reset condition until $V_{DD}$ has reached $V_{POR}$. At this point, the reset condition is released and the PCA9543A/43B registers and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, $V_{DD}$ must be lowered below 0.2 V for at least 5 μs in order to reset the device.

## 6.5 Voltage translation

The pass gate transistors of the PCA9543A/43B are constructed such that the $V_{DD}$ voltage can be used to limit the maximum voltage that will be passed from one I²C-bus to another.




(1) maximum
(2) typical
(3) minimum

**Fig 7. Pass gate voltage versus supply voltage**

Figure 7 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in Section 11 “Static characteristics” of this data sheet). In order for the PCA9543A/43B to act as a voltage translator, the $V_{o(sw)}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{o(sw)}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 7, we see that $V_{o(sw)(max)}$ will be at 2.7 V when the PCA9543A/43B supply voltage is 3.5 V or lower, so the PCA9543A/43B supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 14).

More Information can be found in Application Note *AN262: PCA954X family of I²C/SMBus multiplexers and switches*.


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# 7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

## 7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 8).

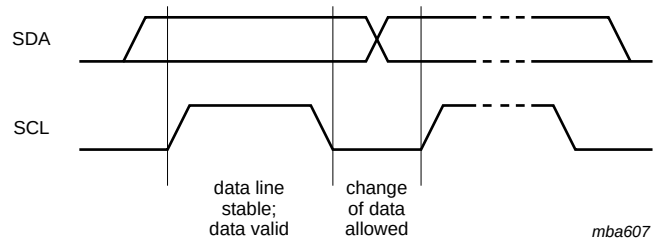



**Fig 8. Bit transfer**

## 7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 9).

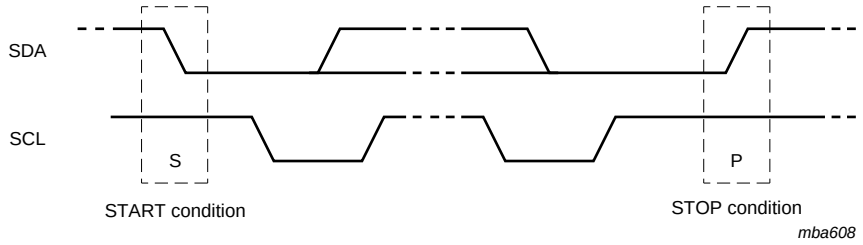



**Fig 9. Definition of START and STOP conditions**


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## 7.3 System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 10).

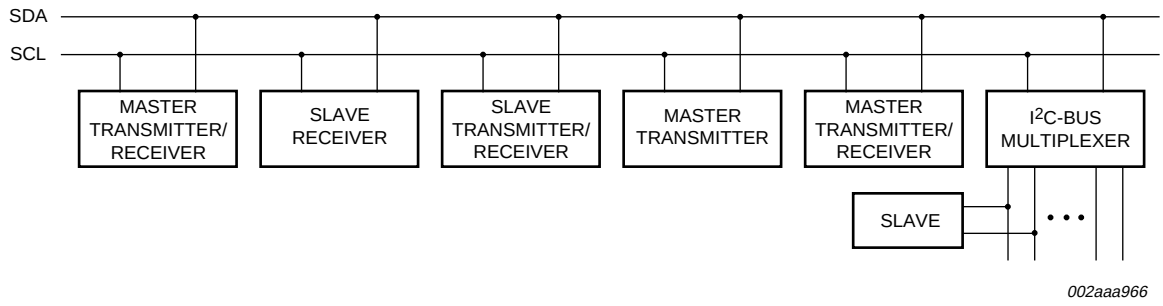



**Fig 10. System configuration**

## 7.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

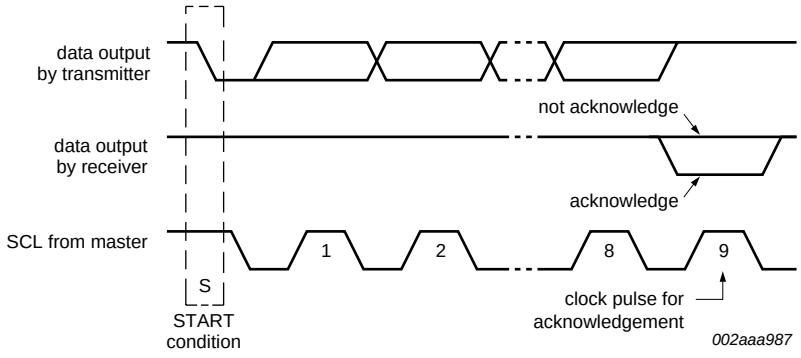



**Fig 11. Acknowledgement on the I²C-bus**


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## 7.5 Bus transactions

Data is transmitted to the PCA9543A/43B control register using the Write mode as shown in Figure 12.

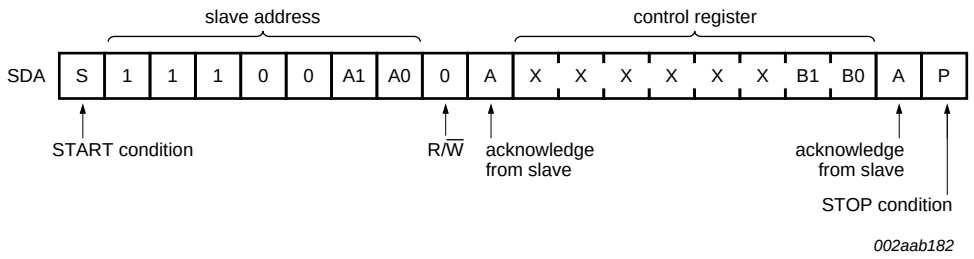



**Fig 12. Write control register**

Data is read from PCA9543A/43B using the Read mode as shown in Figure 13.

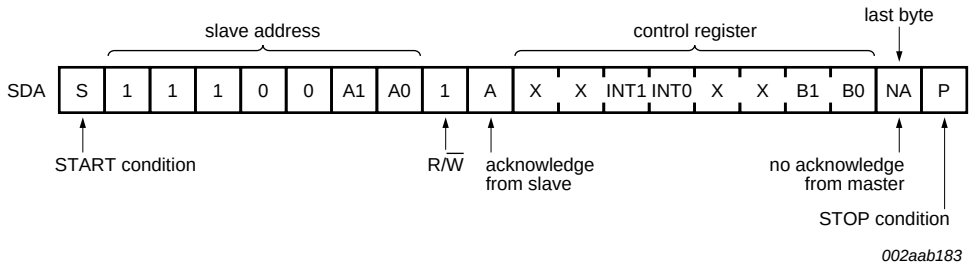
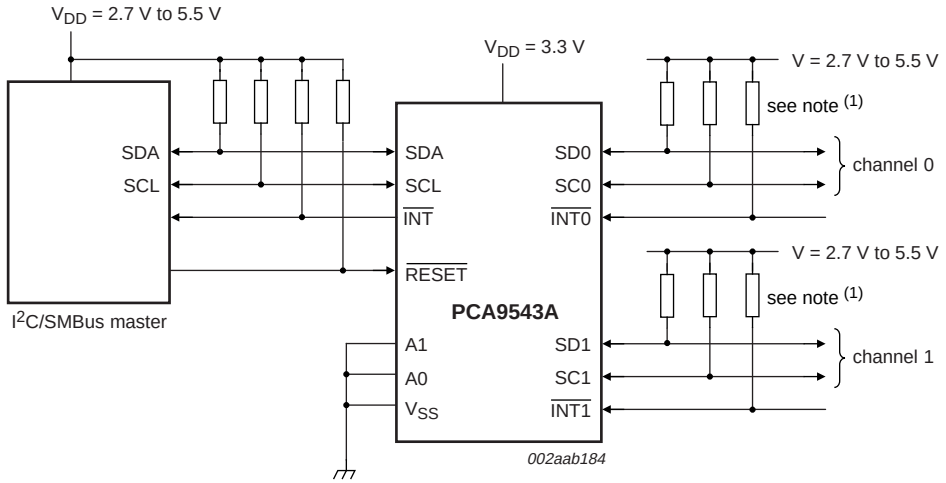



**Fig 13. Read control register**


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# 8. Application design-in information




(1) If the device generating the interrupt has an open-drain output structure or can be 3-stated, a pull-up resistor is required.

If the device generating the interrupt has a totem pole output structure and cannot be 3-stated, a pull-up resistor is not required.

The interrupt inputs should not be left floating.

**Fig 14. Typical application**


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# 9. Limiting values

**Table 8. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS}$ (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | −0.5 | +7.0 | V |
| $V_I$ | input voltage | | −0.5 | +7.0 | V |
| $I_I$ | input current | | - | ±20 | mA |
| $I_O$ | output current | | - | ±25 | mA |
| $I_{DD}$ | supply current | | - | ±100 | mA |
| $I_{SS}$ | ground supply current | | - | ±100 | mA |
| $P_{tot}$ | total power dissipation | | - | 400 | mW |
| $T_{j(max)}$ | maximum junction temperature | [1] | - | 125 | °C |
| $T_{stg}$ | storage temperature | | −60 | +150 | °C |
| $T_{amb}$ | ambient temperature | operating | −40 | +85 | °C |

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

# 10. Thermal characteristics

**Table 9. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | SO14 package | 127 | °C/W |
| | | TSSOP14 package | 175 | °C/W |


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## 11. Static characteristics

**Table 10. Static characteristics at $V_{DD}$ = 2.3 V to 3.6 V**

*$V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified. See Table 11 on page 15 for $V_{DD}$ = 4.5 V to 5.5 V.*[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{DD}$ | supply voltage | | 2.3 | - | 3.6 | V |
| $I_{DD}$ | supply current | operating mode; $V_{DD}$ = 3.6 V; no load; $V_I = V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 100 kHz | - | 40 | 100 | μA |
| $I_{stb}$ | standby current | Standby mode; $V_{DD}$ = 3.6 V; no load; $V_I = V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 0 kHz | - | 0.2 | 1 | μA |
| $V_{POR}$ | power-on reset voltage | no load; $V_I = V_{DD}$ or $V_{SS}$ [2] | - | 1.6 | 2.1 | V |
| **Input SCL; input/output SDA** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | −0.5 | - | +0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7$V_{DD}$ | - | 6 | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | 3 | - | - | mA |
| | | $V_{OL}$ = 0.6 V | 6 | - | - | mA |
| $I_L$ | leakage current | $V_I = V_{DD}$ or $V_{SS}$ | −1 | - | +1 | μA |
| $C_i$ | input capacitance | $V_I = V_{SS}$ | - | 9 | 10 | pF |
| **Select inputs A0, A1, $\overline{INT0}$, $\overline{INT1}$, $\overline{RESET}$** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | −0.5 | - | +0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7$V_{DD}$ | - | 6 | V |
| $I_{LI}$ | input leakage current | $V_I = V_{DD}$ or $V_{SS}$ | −1 | - | +1 | μA |
| $C_i$ | input capacitance | $V_I = V_{SS}$ | - | 1.6 | 3 | pF |
| **Pass gate** | | | | | | |
| $R_{on}$ | ON-state resistance | $V_{DD}$ = 3.0 to 3.6 V; $V_O$ = 0.4 V; $I_O$ = 15 mA | 5 | 11 | 30 | Ω |
| | | $V_{DD}$ = 2.3 V to 2.7 V; $V_O$ = 0.4 V; $I_O$ = 10 mA | 7 | 16 | 55 | Ω |
| $V_{o(sw)}$ | switch output voltage | $V_{i(sw)} = V_{DD}$ = 3.3 V; $I_{o(sw)}$ = −100 μA | - | 1.9 | - | V |
| | | $V_{i(sw)} = V_{DD}$ = 3.0 V to 3.6 V; $I_{o(sw)}$ = −100 μA | 1.6 | - | 2.8 | V |
| | | $V_{i(sw)} = V_{DD}$ = 2.5 V; $I_{o(sw)}$ = −100 μA | - | 1.5 | - | V |
| | | $V_{i(sw)} = V_{DD}$ = 2.5 V to 2.7 V; $I_{o(sw)}$ = −100 μA | 1.1 | - | 2.0 | V |
| $I_L$ | leakage current | $V_I = V_{DD}$ or $V_{SS}$ | −1 | - | +1 | μA |
| $C_{io}$ | input/output capacitance | $V_I = V_{SS}$ | - | 3 | 5 | pF |
| **$\overline{INT}$ output** | | | | | | |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | 3 | - | - | mA |
| $I_{OH}$ | HIGH-level output current | | - | - | +100 | μA |

[1] For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

[2] $V_{DD}$ must be lowered to 0.2 V for at least 5 μs in order to reset part.


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**Table 11. Static characteristics at $V_{DD}$ = 4.5 V to 5.5 V**

*$V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified. See Table 10 on page 14 for $V_{DD}$ = 2.3 V to 3.6 V.*[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{DD}$ | supply voltage | | 4.5 | - | 5.5 | V |
| $I_{DD}$ | supply current | Operating mode; $V_{DD}$ = 5.5 V; no load; $V_I$ = $V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 100 kHz | - | 25 | 100 | μA |
| $I_{stb}$ | standby current | Standby mode; $V_{DD}$ = 5.5 V; no load; $V_I$ = $V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 0 kHz | - | 0.2 | 1 | μA |
| $V_{POR}$ | power-on reset voltage | no load; $V_I$ = $V_{DD}$ or $V_{SS}$ [2] | - | 1.7 | 2.1 | V |
| **Input SCL; input/output SDA** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | −0.5 | - | +0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7$V_{DD}$ | - | 6 | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | 3 | - | - | mA |
| | | $V_{OL}$ = 0.6 V | 6 | - | - | mA |
| $I_L$ | leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | −1 | - | +1 | μA |
| $C_i$ | input capacitance | $V_I$ = $V_{SS}$ | - | 9 | 10 | pF |
| **Select inputs A0, A1, $\overline{INT0}$, $\overline{INT1}$, $\overline{RESET}$** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | −0.5 | - | +0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7$V_{DD}$ | - | 6 | V |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | −1 | - | +50 | μA |
| $C_i$ | input capacitance | $V_I$ = $V_{SS}$ | - | 2 | 5 | pF |
| **Pass gate** | | | | | | |
| $R_{on}$ | ON-state resistance | $V_{DD}$ = 4.5 V to 5.5 V; $V_O$ = 0.4 V; $I_O$ = 15 mA | 4 | 9 | 24 | Ω |
| $V_{o(sw)}$ | switch output voltage | $V_{i(sw)}$ = $V_{DD}$ = 5.0 V; $I_{o(sw)}$ = −100 μA | - | 3.6 | - | V |
| | | $V_{i(sw)}$ = $V_{DD}$ = 4.5 V to 5.5 V; $I_{o(sw)}$ = −100 μA | 2.6 | - | 4.5 | V |
| $I_L$ | leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | −1 | - | +100 | μA |
| $C_{io}$ | input/output capacitance | $V_I$ = $V_{SS}$ | - | 3 | 5 | pF |
| **$\overline{INT}$ output** | | | | | | |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | 3 | - | - | mA |
| $I_{OH}$ | HIGH-level output current | | - | - | +100 | μA |

[1] For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

[2] $V_{DD}$ must be lowered to 0.2 V for at least 5 μs in order to reset part.


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## 12. Dynamic characteristics

**Table 12. Dynamic characteristics**

| Symbol | Parameter | Conditions | Standard-mode I²C-bus | | Fast-mode I²C-bus | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PD}$ | propagation delay | from SDA to SDx, or SCL to SCx | - | 0.3[1] | - | 0.3[1] | ns |
| $f_{SCL}$ | SCL clock frequency | | 0 | 100 | 0 | 400 | kHz |
| $t_{BUF}$ | bus free time between a STOP and START condition | | 4.7 | - | 1.3 | - | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition | [2] | 4.0 | - | 0.6 | - | µs |
| $t_{LOW}$ | LOW period of the SCL clock | | 4.7 | - | 1.3 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | 4.0 | - | 0.6 | - | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | 4.7 | - | 0.6 | - | µs |
| $t_{SU;STO}$ | set-up time for STOP condition | | 4.0 | - | 0.6 | - | µs |
| $t_{HD;DAT}$ | data hold time | | 0[3] | 3.45 | 0[3] | 0.9 | µs |
| $t_{SU;DAT}$ | data set-up time | | 250 | - | 100 | - | ns |
| $t_r$ | rise time of both SDA and SCL signals | | - | 1000 | $20 + 0.1C_b$[4] | 300 | ns |
| $t_f$ | fall time of both SDA and SCL signals | | - | 300 | $20 + 0.1C_b$[4] | 300 | ns |
| $C_b$ | capacitive load for each bus line | | - | 400 | - | 400 | pF |
| $t_{SP}$ | pulse width of spikes that must be suppressed by the input filter | | - | 50 | - | 50 | ns |
| $t_{VD;DAT}$ | data valid time | HIGH-to-LOW [5] | - | 1 | - | 1 | µs |
| | | LOW-to-HIGH [5] | - | 0.6 | - | 0.6 | µs |
| $t_{VD;ACK}$ | data valid acknowledge time | | - | 1 | - | 1 | µs |
| **$\overline{INT}$** | | | | | | | |
| $t_{v(INTnN-INTN)}$ | valid time from $\overline{INTn}$ to $\overline{INT}$ signal | | - | 4 | - | 4 | µs |
| $t_{d(INTnN-INTN)}$ | delay time from $\overline{INTn}$ to $\overline{INT}$ inactive | | - | 2 | - | 2 | µs |
| $t_{w(rej)L}$ | LOW-level rejection time | $\overline{INTn}$ inputs | 1 | - | 1 | - | µs |
| $t_{w(rej)H}$ | HIGH-level rejection time | $\overline{INTn}$ inputs | 0.5 | - | 0.5 | - | µs |
| **$\overline{RESET}$** | | | | | | | |
| $t_{w(rst)L}$ | LOW-level reset time | | 4 | - | 4 | - | ns |
| $t_{rst}$ | reset time | SDA clear | 500 | - | 500 | - | ns |
| $t_{REC;STA}$ | recovery time to START condition | | 0 | - | 0 | - | ns |

[1] Pass gate propagation delay is calculated from the 20 Ω typical $R_{on}$ and the 15 pF load capacitance.

[2] Hold time (repeated) START condition. After this period, the first clock pulse is generated.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4] $C_b$ = total capacitance of one bus line in pF.

[5] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.


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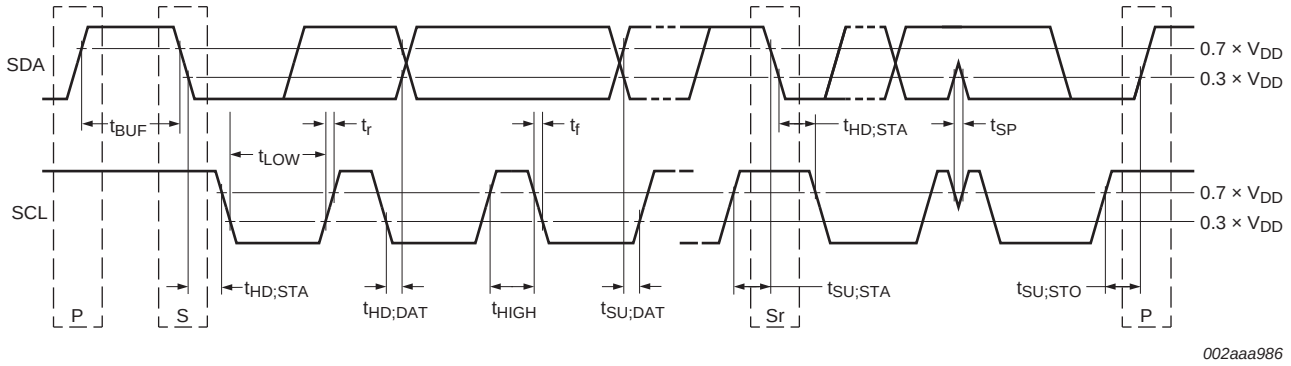



**Fig 15. Definition of timing on the I²C-bus**

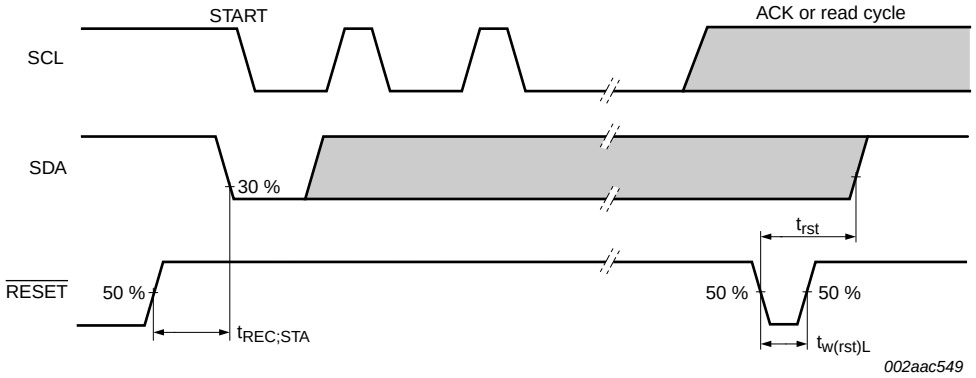
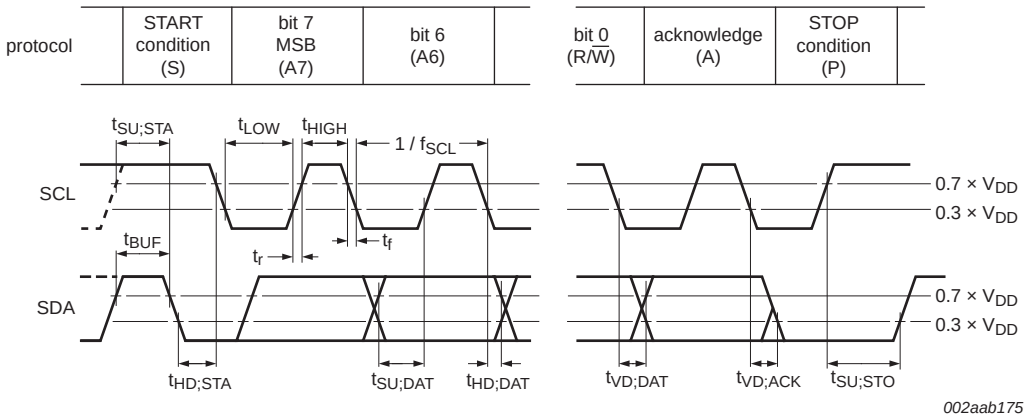



**Fig 16. Definition of $\overline{\text{RESET}}$ timing**




Rise and fall times refer to $V_{IL}$ and $V_{IH}$.

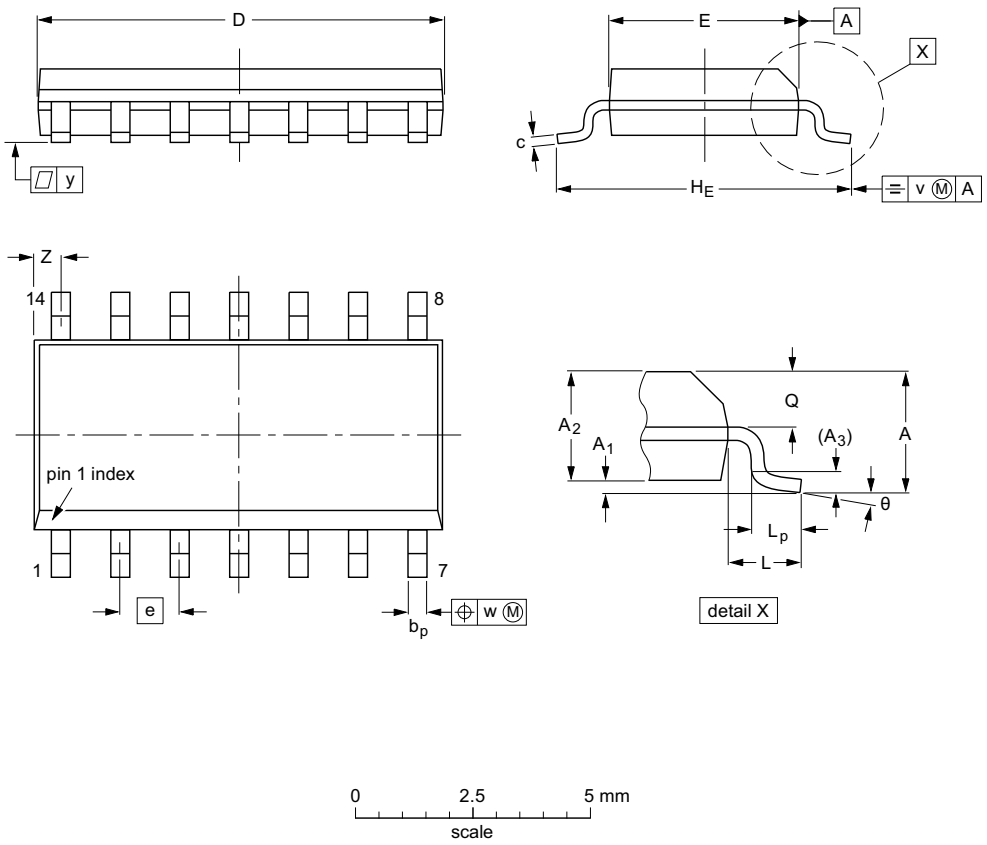
**Fig 17. I²C-bus timing diagram**


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## 13. Package outline

**SO14: plastic small outline package; 14 leads; body width 3.9 mm** **SOT108-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 8.75<br>8.55 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.35<br>0.34 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

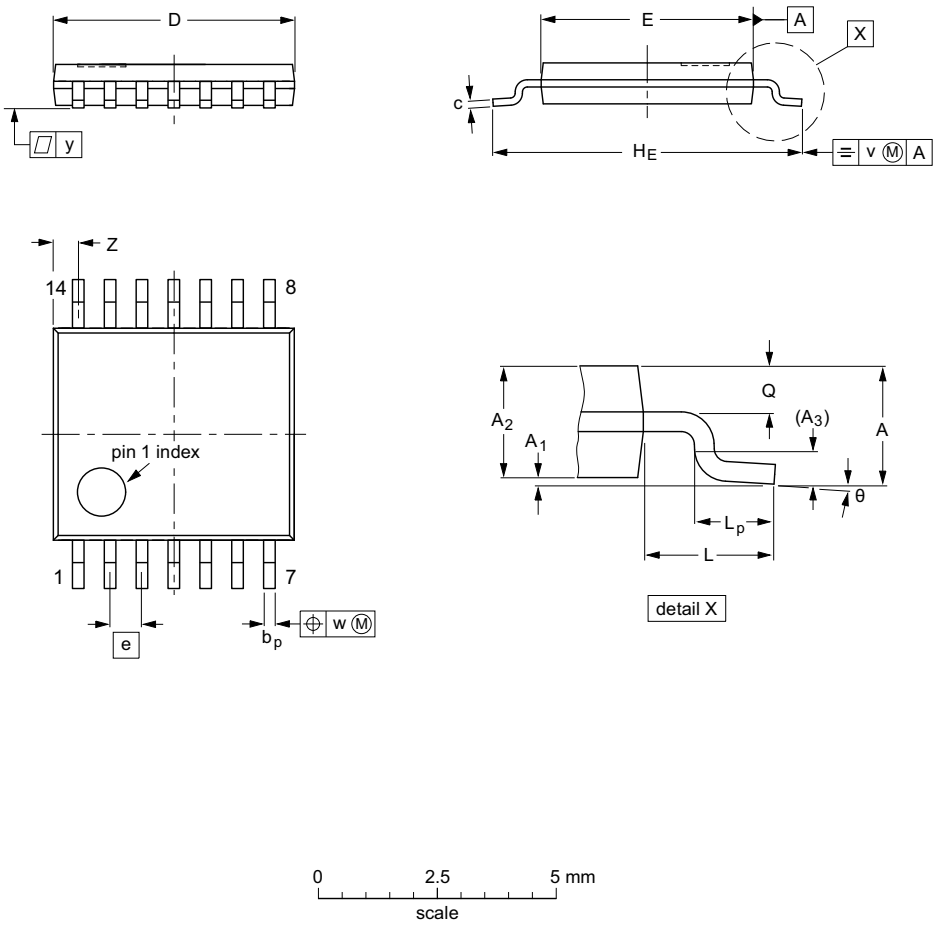
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT108-1 | 076E06 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 18. Package outline SOT108-1 (SO14)**


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**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm** **SOT402-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 19. Package outline SOT402-1 (TSSOP14)**


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# 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities


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## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

**Table 13. SnPb eutectic process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume (mm³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 14. Lead-free process (from J-STD-020D)**

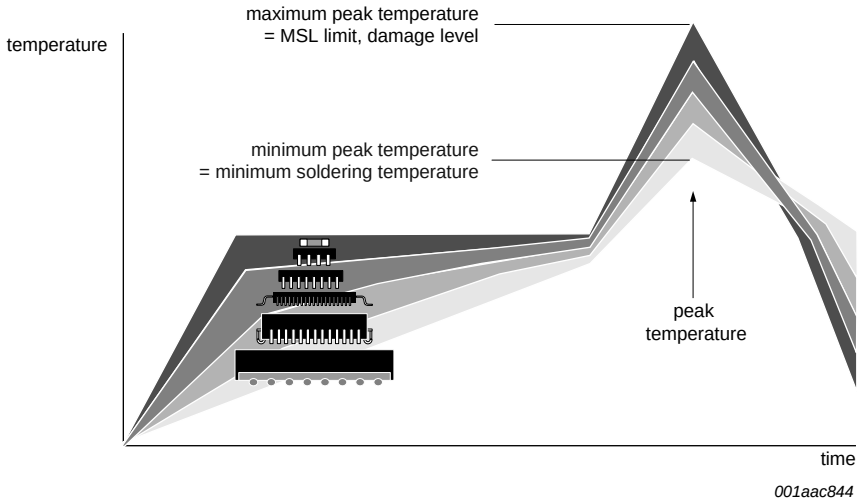
| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume (mm³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.


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MSL: Moisture Sensitivity Level

**Fig 20. Temperature profiles for large and small components**

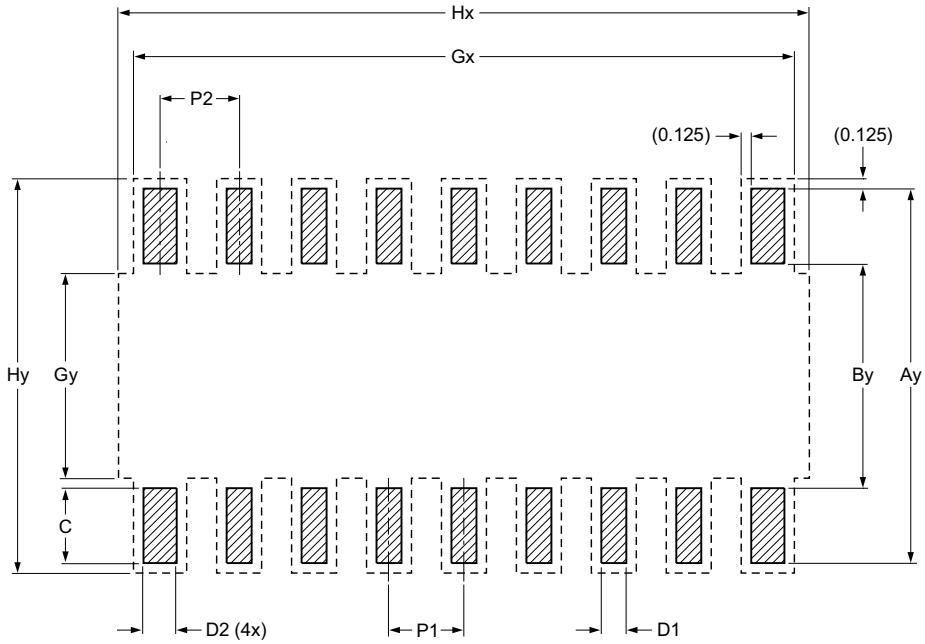
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.


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## 15. Soldering: PCB footprints

**Footprint information for reflow soldering of SO14 package** **SOT108-1**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

| P1 | P2 | Ay | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|
| 1.270 | 1.320 | 7.400 | 3.900 | 1.750 | 0.700 | 0.800 | 8.770 | 5.200 | 11.900 | 7.650 |

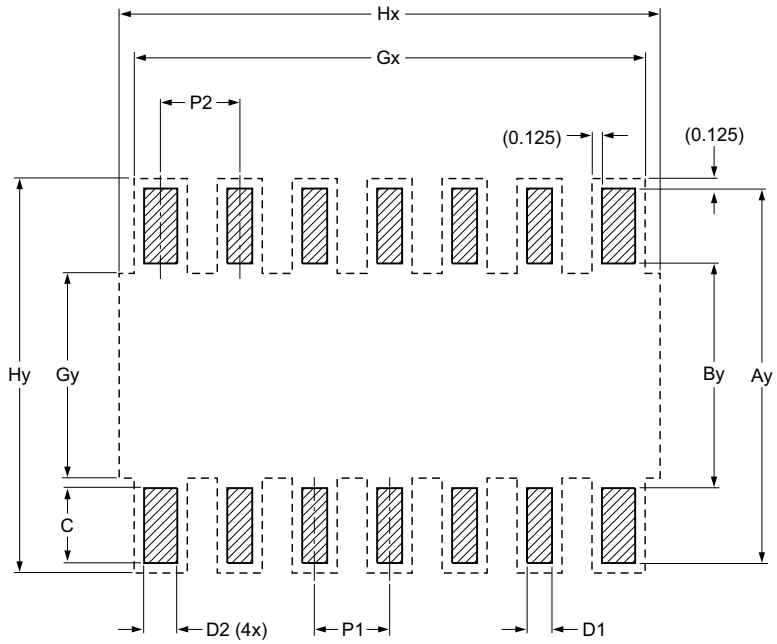
*sot108-1_fr*

**Fig 21. PCB footprint for SOT108-1 (SO14); reflow soldering**


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**Footprint information for reflow soldering of TSSOP14 package** **SOT402-1**




Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

| P1 | P2 | Ay | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|
| 0.650 | 0.750 | 7.200 | 4.500 | 1.350 | 0.400 | 0.600 | 4.950 | 5.300 | 5.800 | 7.450 |

*sot402-1_fr*

**Fig 22. PCB footprint for SOT402-1 (TSSOP14); reflow soldering**


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# 16. Abbreviations

**Table 15. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged-Device Model |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| IC | Integrated Circuit |
| I²C-bus | Inter-Integrated Circuit bus |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| PCB | Printed-Circuit Board |
| SMBus | System Management Bus |

# 17. Revision history

**Table 16. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCA9543A_43B v.8 | 20140403 | Product data sheet | - | PCA9543A_43B v.7 |
| Modifications: | • Figure 6 “Control register” updated: corrected label above bits [7:4] from “(read only)” to “(read/write) but reads back chip status; bit 6 and bit 7 always read 0”<br>• Section 6.2.1 “Control register definition”: added second paragraph<br>• Section 6.2.2 “Interrupt handling”:<br>– Table 7 “Control register: Read — interrupt” corrected: bits [7:6] corrected from “XX” to “00” (for both channel 0 and channel 1)<br>– ‘Remark’ paragraph: added second sentence<br>• Section 6.4 “Power-on reset”, first paragraph, third sentence corrected from “Thereafter, $V_{DD}$ must be lowered below 0.2 V to reset the device.” to “Thereafter, $V_{DD}$ must be lowered below 0.2 V for at least 5 μs in order to reset the device.”<br>• Table 10 “Static characteristics at $V_{DD}$ = 2.3 V to 3.6 V”, Table note [2]: inserted phrase “for at least 5 μs”<br>• Table 11 “Static characteristics at $V_{DD}$ = 4.5 V to 5.5 V”, Table note [2]: inserted phrase “for at least 5 μs” | | | |
| PCA9543A_43B v.7 | 20130228 | Product data sheet | - | PCA9543A_43B_43C v.6 |
| PCA9543A_43B_43C v.6 | 20090615 | Product data sheet | - | PCA9543A_43B_43C v.5 |
| PCA9543A_43B_43C v.5 | 20081117 | Product data sheet | - | PCA9543A_43B_43C v.4 |
| PCA9543A_43B_43C v.4 | 20061020 | Product data sheet | - | PCA9543A v.3 |
| PCA9543A v.3 (9397 750 14316) | 20050321 | Product data sheet | - | PCA9543A v.2 |
| PCA9543A v.2 (9397 750 13988) | 20040929 | Objective data sheet | - | PCA9543A v.1 |
| PCA9543A v.1 (9397 750 13299) | 20040728 | Objective data sheet | - | - |


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# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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For more information, please visit: **http://www.nxp.com**

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## 20. Contents


**1 General description . . . . . 1**
**2 Features and benefits . . . . . 1**
**3 Ordering information . . . . . 2**
3.1 Ordering options . . . . . 2
**4 Block diagram . . . . . 3**
**5 Pinning information . . . . . 4**
5.1 Pinning . . . . . 4
5.2 Pin description . . . . . 4
**6 Functional description . . . . . 5**
6.1 Device address . . . . . 5
6.1.1 Address maps . . . . . 5
6.2 Control register . . . . . 6
6.2.1 Control register definition . . . . . 6
6.2.2 Interrupt handling . . . . . 7
6.3 RESET input . . . . . 7
6.4 Power-on reset . . . . . 8
6.5 Voltage translation . . . . . 8
**7 Characteristics of the I²C-bus . . . . . 9**
7.1 Bit transfer . . . . . 9
7.2 START and STOP conditions . . . . . 9
7.3 System configuration . . . . . 10
7.4 Acknowledge . . . . . 10
7.5 Bus transactions . . . . . 11
**8 Application design-in information . . . . . 12**
**9 Limiting values . . . . . 13**
**10 Thermal characteristics . . . . . 13**
**11 Static characteristics . . . . . 14**
**12 Dynamic characteristics . . . . . 16**
**13 Package outline . . . . . 18**
**14 Soldering of SMD packages . . . . . 20**
14.1 Introduction to soldering . . . . . 20
14.2 Wave and reflow soldering . . . . . 20
14.3 Wave soldering . . . . . 20
14.4 Reflow soldering . . . . . 21
**15 Soldering: PCB footprints . . . . . 23**
**16 Abbreviations . . . . . 25**
**17 Revision history . . . . . 25**
**18 Legal information . . . . . 26**
18.1 Data sheet status . . . . . 26
18.2 Definitions . . . . . 26
18.3 Disclaimers . . . . . 26
18.4 Trademarks . . . . . 27
**19 Contact information . . . . . 27**
**20 Contents . . . . . 28**


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